## BD95700MUV

## - Description

BD95700MUV is a 2 phase switching regulator controller with high output current which can achieve low output voltage ( 0.4 V ~ 3.3 V ) from AC/DC 5 V or 12 V . High efficiency for the switching regulator can be realized by utilizing an external N-MOSFET power transistor. A new technology called $\mathrm{H}^{3} \mathrm{Reg}^{\mathrm{TM}}$ is a Rohm proprietary control method to realize ultra high transient response against load change without phase compensation capacitance and resistance. For various applications, it is available to select the 3 types of N-MOSFET gate drive voltage ( 12 V : for drive ability, 8 V : for intermediate drive ability, 5 V : for small real estate).

## - Features

1) $\mathrm{H}^{3} \mathrm{Reg}^{\mathrm{TM}}$ Switching Regulator Controller without phase compensation capacitance and resistance
2) Ultra High Tolerance Internal Reference Voltage (+/- 1\%)
3) Thermal Shut Down (TSD), Under Voltage LockOut (UVLO), Adjustable Over Current Protection (OCP), Over Voltage Protection (OVP), Short Circuit protection(SCP) built-in
4) Soft start function to minimize rush current during startup
5) Switching Frequency Variable ( $\mathrm{f}=50 \mathrm{kHz} \sim 1000 \mathrm{kHz}$ )
6) Internal Bootstrap Diode
7) High Tolerance Current Balance Function
8) VQFN024V4040 Package $(4.0 \mathrm{~mm} \times 4.0 \mathrm{~mm} \times 1.0 \mathrm{~mm})$
9) Integrated 1-/2-phase Switching Function
-Applications
Graphic Cards, Desktop PC, Gaming Equipments, Digital Components

- Maximum Absolute Ratings ( $\mathrm{Ta}=25^{\circ} \mathrm{C}$ )

| Parameter | Symbol | Limit | Unit |
| :--- | :---: | :---: | :---: |
| Input Voltage 1 | VCC | $15^{* 1}$ | V |
| Input Voltage 2 | VIN | $15^{* 1}$ | V |
| Input Voltage 3 | VCCDRV | $15^{{ }^{1} 1}$ | V |
| Input Voltage 4 | 5VCC | $7^{* 1}$ | V |
| Input Voltage 5 | REFIN | $7^{* 1{ }^{*} 2}$ | V |
| Input Voltage 6 | BUSEN | $7^{* 1}$ | V |
| BOOT Voltage | BOOT1, BOOT2 | $30^{* 1}$ | V |
| BOOT-SW Voltage | BOOT-SW | $15^{* 1}$ | V |
| UG-SW Voltage | UG-SW | $15^{* 1}$ | V |
| SW Voltage | SW | 15 | V |
| Power Dissipation | Pd1 | 0.34 | W |
| Operating Temperature Range | Topr | $0 \sim+70$ | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | Tstg | $-55 \sim+150$ | ${ }^{\circ} \mathrm{C}$ |
| Junction Temperature | Tjmax | +150 | ${ }^{\circ} \mathrm{C}$ |

*1 Do not to exceed Pd.
*2 REFIN voltage can not go up higher than 5VCC voltage.

- Operating Conditions $\left(\mathrm{Ta}=25^{\circ} \mathrm{C}\right)$

| Parameter | Symbol | MIN | MAX | Unit |
| :--- | :---: | :---: | :---: | :---: |
| Input Voltage 1 | VCC | 4.7 | 13.2 | V |
| Input Voltage 2 | VIN | 3.3 | 13.2 | V |
| Input Voltage 5 | REFIN | 0.4 | 3.3 | V |
| Input Voltage 6 | BUSEN | 0 | 3.3 | V |
| BOOT Voltage | BOOT | 4.5 | 27 | V |
| BOOT-SW Voltage | BOOT-SW | 4.5 | 13.2 | V |
| CS Input Voltage | CS1-/CS1+/CS2-/CS2+ | 0.4 | 3.3 | V |
| DROOP Setting Resistor | $\mathrm{R}_{\text {DROOP }}$ | 0 | 510 k | $\Omega$ |
| IOUT Setting Resistor | $\mathrm{R}_{\text {IOUT }}$ | 0 | 5 M | $\Omega$ |
| RT Setting Resistor | $\mathrm{R}_{\text {RT }}$ |  | 10 k | 510 k |

[^0]- ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $\mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{VCC}=5 \mathrm{~V}, \mathrm{VIN}=12 \mathrm{~V}, \mathrm{REF}=1.2 \mathrm{~V}, \mathrm{RT}=100 \mathrm{k} \Omega$ )

| Parameter | Symbol | Standard Value |  |  | Unit | Condition |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | TYP | MAX |  |  |
| [Total Block] |  |  |  |  |  |  |
| Vcc Bias Current | Icc | - | 4 | 10 | mA |  |
| Vcc Standby Current | $\mathrm{I}_{\text {STB }}$ | - | 1.5 | 2.0 | mA |  |
| [5Vcc Block] |  |  |  |  |  |  |
| 5 Vcc Output Voltage | 5 Vcc | 4.9 | 5 | 5.1 | V |  |
| 5 Vcc Output Current | $\mathrm{I}_{5 \mathrm{Vcc}}$ | 20 | - | - | mA |  |
| [UVLO Block] |  |  |  |  |  |  |
| VCC Threshold Voltage | Vcc_UVLO | 4.2 | 4.5 | 4.7 | V | Low $\rightarrow$ High |
| VCC Hysteresis Voltage | dVcc_UVLO | 130 | 180 | 230 | mV |  |
| BUS EN Threshold Voltage | BUS_UVLO | 0.6 | 0.8 | 0.9 | V | Low $\rightarrow$ High |
| BUS EN Hysteresis Voltage | dBUS_UVLO | 5 | 25 | 50 | mV |  |
| 5Vcc Threshold Voltage | 5Vcc_UVLO | 4.1 | 4.3 | 4.5 | V | Low $\rightarrow$ High |
| 5 Vcc Hysteresis Voltage | dVcc_UVLO | 100 | 150 | 200 | mV |  |
| [Reference Voltage Block] |  |  |  |  |  |  |
| Internal Reference Voltage | $\mathrm{V}_{\text {REF }}$ | 0.594 | 0.600 | 0.606 | V | REFIN=5VCC |
| REFIN Offset Voltage | $\mathrm{V}_{\text {REFIN }}$ | REF_IN-10m | REF_IN | REF_IN+10m | V |  |
| REFIN Input Voltage Range | $V_{\text {REF }}$ | 0.4 | - | 3.3 | V |  |
| REFIN Off Threshold Voltage | $\mathrm{V}_{\text {th ReFIN }}$ | 4.5 | - | 5 Vcc | V |  |
| [EN Threshold] |  |  |  |  |  |  |
| EN Low voltage | Enlow | GND | - | 0.3 | V | REFIN pin voltage input |
| EN High voltage | Enhigh | 0.4 | - | 5 Vcc | V | REFIN pin voltage input |
| [Operating Frequency] |  |  |  |  |  |  |
| Oscillation Frequency | Fosc | - | 500 | - | kHz |  |
| ON Time | Ton | 100 | 200 | 300 | nsec |  |
| MIN OFF Time | Toffmin | - | 400 | 500 | nsec |  |
| [IREFOUT voltage Block] |  |  |  |  |  |  |
| IREFOUT Voltage | $\mathrm{V}_{\text {IReFout }}$ | 1.176 | 1.2 | 1.224 | V |  |
| IREFOUT Drive Current | I IREFOUT | 3 | 5 | - | mA |  |
| [FET Gate Driver Block] |  |  |  |  |  |  |
| UG high side ON Resistance | $\mathrm{R}_{\text {onHGH }}$ | - | 6 | 12 | $\Omega$ |  |
| UG low side ON Resistance | $\mathrm{R}_{\text {onHGL }}$ | - | 4 | 8 | $\Omega$ |  |
| LG high side ON Resistance | $\mathrm{R}_{\text {onLGH }}$ | - | 6 | 12 | $\Omega$ |  |
| LG high side ON Resistance | $\mathrm{R}_{\text {onLGL }}$ | - | 1 | 2 | $\Omega$ |  |
| [Regulator for VCC] |  |  |  |  |  |  |
| Output Voltage | VCCDRV | 7.2 | 8 | 8.8 | V |  |
| Vcc DRV Drive Current | IvcCDRv | - | 10 | - | mA |  |
| [Droop Block] |  |  |  |  |  |  |
| Load Line Slope | SLOPE ${ }_{\text {LL }}$ | - | 40 | - | nA | $\mathrm{DCR}=5 \mathrm{~m} \Omega$ |
| Load Line Slope Gain | SLOPEGAIN | 0.75 | 0.8 | 0.85 |  |  |
| [OCP (Over Current Protection) Block] |  |  |  |  |  |  |
| Over Current Threshold | $\mathrm{OCP}_{\text {TH }}$ | 0.95 | 1 | 1.05 | V |  |
| [OVP (Over Voltage Protection) Block] |  |  |  |  |  |  |
| Over Voltage Threshold 1 | $\mathrm{OVP}_{\text {TH1 }}$ | VREFx1.25 | VREFx1.3 | VREFx1.35 | V | REFIN=5Vcc |
| Over Voltage Threshold 2 | OVP ${ }_{\text {TH2 }}$ | REFINx1.25 | REFINx1.3 | REFINx1.35 | V |  |
| [SCP (Short Circuit Protection) Block] |  |  |  |  |  |  |
| SCP Start up Voltage 1 | $\mathrm{V}_{\text {ScP }} 1$ | VREFx0.45 | VREFx0.5 | VREFx0.55 | V | REFIN=5Vcc |
| SCP Start up Voltage 2 | $\mathrm{V}_{\text {ScP }} 2$ | REFINx0.45 | REFINx0.5 | REFINx0.55 | V |  |
| SCP Delay Time | Tscp | - | 1 | - | ms |  |
| [POK Detection Block] |  |  |  |  |  |  |
| POK Threshold 1 | $\mathrm{POK}_{\text {THLOW1 }}$ | VREFx0.7 | VREFx0.75 | VREFx0.80 | V | REFIN=5Vcc |
| POK Threshold 2 | $\mathrm{POK}_{\text {THLOW2 }}$ | VREFINx0.70 | VREFINx0.75 | VREFINx0.80 | V |  |

* Design Guarantee

-Pin Configuration

-Pin Function Table

| PIN No. | PIN Name | PIN Function |
| :---: | :---: | :---: |
| 1 | UG1 | High Side FET Gate Drive Pin 1 |
| 2 | BT1 | Supply Voltage for UG1 |
| 3 | 5VCC | 5V Regulator Output (lomin=20mA) |
| 4 | AGND | Sense GND |
| 5 | BUSEN | Bus Enable, Power Supply Monitoring Pin |
| 6 | CS1+ | Positive Input of Current Sensing 1 |
| 7 | CS1- | Negative Input of Current Sensing 1 |
| 8 | CS2- | Negative Input of Current Sensing 2 |
| 9 | CS2+ | Positive Input of Current Sensing 2 |
| 10 | IMAX / IOUT | Current Limit/Output Current Indication |
| 11 | RT | Switching Frequency Setting |
| 12 | DROOP | Droop Control of the Load Line |
| 13 | FB | Output Voltage Feedback Pin |
| 14 | PGND | Power GND Pin |
| 15 | REFIN/ EN | External Reference Input and Enable Pin |
| 16 | INREFOUT/ POK | Internal Reference Voltage Output and Power Good Output Pin |
| 17 | BT2 | Supply Voltage for UG2 |
| 18 | UG2 | High Side FET Gate Drive Pin 2 |
| 19 | SW2 | Switch Node for Channel 2 |
| 20 | LG2 | Low Side FET Gate Drive Pin 2 |
| 21 | VCCDRV | Driver for External Linear Regulator |
| 22 | VCC | Supply Voltage Pin |
| 23 | LG1 | Low Side FET Gate Drive Pin 1 |
| 24 | SW1 | Switch Node for Channel 1 |
| Exposed Pad |  | FIN |

-Pin Descriptions

- UG1 (Pin 1), UG2 (Pin 18)

These are the voltage supply pins to drive the Gate of the high side FET. This voltage swings between BT1/2 and SW1/2. High-speed Gate driving for the high side FET is achieved due to the low on-resistance ( 3 ohm when UG is high, 2 ohm when UG is low) of the driver.

- BT1 (Pin 2), BT2 (Pin 17)

These are the voltage supply pins to drive the high side FET. The maximum absolute ratings are 35 V (from GND) and 15 V (from SW1/2). BT1/2 voltages swing between VIN+VCC and VCC during active operation.

- 5VCC (Pin 3)

This is the internal 5 V regulator output pin. The minimum output current capability is 20 mA .

- AGND (Pin 4)

This is the ground pin for IC internal circuits. It is equivalent to FIN voltage.

- BUSEN (Pin 5)

This pin monitors the supply input VIN through resistance divider. The POR rising threshold level is set to 0.8 V .

- Cs1+ (Pin 6), Cs2+ (Pin 9), Cs1- (Pin 7), Cs2- (Pin 8)

These pins are connected to both sides of the current sense resistance or Inductance (DCR sensing) to detect output current.

- IMAX / IOUT (Pin 10)

This pin has multiple functions such as the output current indication, OCP (Over Current Protection) limit setting, and the output voltage load line adjustment pin. BD95700MUV detects the voltage between Cs+ pin and Cs- pin and limits the output current (OCP) using resistance connected between IMAX/IOUT/Droop and GND. A very low current sense resistor or inductor DCR can also be used for this platform.

- RT (Pin 11)

This is the pin to adjust the switching frequency based on the resistance value. The frequency range is $\mathrm{f}=50 \mathrm{KHz}-1000 \mathrm{KHz}$.

- DROOP (Pin 12)

This pin can be used for the load slope setting of the output voltage.

- FB (Pin 13)

This is the output voltage feedback pin. It is possible to adjust the output voltage using external resistor divider based on the equation, REFIN $\fallingdotseq F B$. However, $F B$ becomes 0.6 V when $\mathrm{REFIN}=5 \mathrm{VCC}$.

- PGND (Pin 14)

This is the power ground pin connected to the source of the low side FET.

- REFIN/EN (Pin 15)

This is an internal or external reference voltage selectable pin. If REFIN is pulled up to 5 VCC , internal reference voltage ( 0.6 V ) is used. If REFIN is driven by an external voltage ranged 0.4 V to 3.3 V , external voltage of REFIN voltage is used. It is very convenient for synchronizing external voltage supply. The IC controls the output voltage (REFIN $\fallingdotseq$ FB). And also this pin is used for enable function. If REFIN is less than 0.3 V , the whole circuit is shut down.

- IREFOUT/POK (Pin 16)

This pin is internal reference voltage output and power good output. During start up, this pin voltage is low. This pin becomes high impedance when FB pin voltage goes beyond $75 \%$ of specified FB voltage after soft start ends.

- SW1 (Pin 24), SW2 (Pin 19)

These are the source pins for the high side FET. The maximum absolute ratings are 15 V (from GND). SW1/2 voltage swings between VIN and GND.

- LG1 (Pin 23), LG2 (Pin 20)

This is the voltage supply to drive the Gate of the low side FET. This voltage swings between VCC and PGND. High-speed Gate driving for the low side FET is achieved due to the low on-resistance ( 2 ohm when LG1/2 is high, 0.5 ohm when LG1/2 is low) of the driver.

- VCCDRV (Pin 21)

This is the supply voltage pin to drive an external NPN/N_MOSFET for 8 V linear regulator. The maximum absolute rating is 15V.

- VCC (Pin 22)

This is the power supply pin for IC internal circuit and driver circuit. The maximum circuit current is 10 mA . There are 3 usages depending on a supply voltage for driver ( $5 \mathrm{~V}, 8 \mathrm{~V}$, and 12 V ). It is recommended that a 0.1 uF bypass capacitor be put in this pin to avoid voltage fluctuation when the VCC is supplied from 5 V or 12 V rail directly from the actual platforms. If 8 V is used for the supply voltage, this pin is connected to the LDO output. In this case, it is recommended that at least 10uF ceramic capacitor be input to avoid oscillation.

## - Explanation of Operation

The BD95700MUV is a synchronous buck regulator controller incorporating ROHM's proprietary $\mathrm{H}^{3} \mathrm{Reg}^{\text {TM }}$ CONTROLLA control system. When Vout drops due to a rapid load change, the system quickly restores Vout by extending the Ton time interval. Thus, it serves to improve the regulator's transient response.
$\mathrm{H}^{3} \mathrm{Reg}^{\mathrm{TM}}$ control
(Normal operation)


When FB pin voltage (Vout) falls to a threshold voltage REF, the drop is detected, activating the $\mathrm{H}^{3} \mathrm{Reg}^{\mathrm{TM}}$ CONTROLLA system.

$$
\text { TON }=\frac{\text { REF }}{\text { VIN }} \times \frac{1}{\mathrm{f}}[\mathrm{sec}] \cdots(1)
$$

UG output is determined with the formula above.
LG outputs until the status of VOUT is lower than REF after the status of UG is off.

Note: REF is an internal or external reference voltage. If the internal reference is utilized, $\mathrm{REF}=0.6 \mathrm{~V}$. If the external reference is utilized, REF = REFIN pin voltage.

Phase switch function


The IC normally operates in 2-phase mode, but when the input voltage on the VIN_EXT pin is cut off, the IC latches into single-phase mode. The IC will remain latched in this mode (even if a voltage is reintroduced onto the VIN_EXT pin) until the voltage is cycled on any of the EN, VCC or BUSEN pins. It will then return to two-phase mode.

Timing Chart

- Soft Start Function

- Output Over Voltage Protection

- Short Circuit Protection with Timer Latch


Soft start is activated when REF hits its enabling threshold (VCC, 5VCC, and BUSEN have to be beyond their own UVLO thresholds). Current control takes effect at startup, enabling an output voltage "ramping start." Soft start timing and incoming current are calculated with formulas (2) and below.

Soft start time $($ TSS $) \fallingdotseq 3 \mathrm{msec}($ fixed $)$
Incoming current
$\mathrm{IIN}=\frac{\mathrm{Co} \times \mathrm{VOUT}}{3 \mathrm{msec}}[\mathrm{A}] \cdot \cdot(2)$
(Co: Output capacitor)

When the FB pin voltage becomes REF x 1.3, the output over voltage protection is activated and Low side MOSFET becomes ON to lower the output voltage (LG=High, UG=Low). When the output voltage goes back down to the specified level, the whole circuit becomes the normal operation mode.

Short Circuit Protection kicks in when output falls to or below REF x 0.5 . When the programmed time period elapses, output is latched OFF to prevent destruction of the IC. Output voltage can be restored either by reconnecting the REFIN pin (ON $\rightarrow$ OFF $\rightarrow$ ON) or disabling UVLO (HIGH $\rightarrow$ Low $\rightarrow$ High).

External Component Selection

1. Inductor (L) selection


Output Ripple Current

The inductor value is a major influence on the output ripple current. As formula (3) below indicates, the greater the inductor or the switching frequency, the lower the ripple current.

$$
\Delta \mathrm{IL}=\frac{(\mathrm{VIN}-\mathrm{VOUT}) \times \mathrm{VOUT}}{\mathrm{~L} \times \mathrm{VIN} \times \mathrm{f}} \quad[\mathrm{~A}] \cdot \cdot \cdot(3)
$$

The proper output ripple current setting is about $30 \%$ of maximum output current.

$$
\begin{aligned}
\Delta \mathrm{IL} & =0.3 \times \text { IOUTmax } / 2 .[\mathrm{A}] \cdot \cdots(4) \\
\mathrm{L} & =\frac{(\mathrm{VIN}-\mathrm{VOUT}) \times \mathrm{VOUT}}{\Delta \mathrm{IL} \times \mathrm{VIN} \times \mathrm{f}}[\mathrm{H}] \cdot \cdots(5)
\end{aligned}
$$

( $\Delta \mathrm{IL}$ : output ripple current; f: switch frequency)
※Passing a current larger than the inductor's rated current will cause magnetic saturation in the inductor and decrease system efficiency. In selecting the inductor, be sure to allow enough margin to assure that peak current does not exceed the inductor rated current value.
※To minimize possible inductor damage and maximize efficiency, choose a inductor with a low (DCR, ACR) resistance.
2. Output Capacitor (Co) Selection


Output Capacitor

At least 20 mV ripple voltage of the FB voltage is recommended by taking the equivalent series resistance and inductance into account.

Output ripple voltage is determined as in formula (6) below.
$\Delta V O U T=\Delta I L \times E S R+E S L \times \Delta I L / T O N \cdot \cdots(6)$
( $\Delta \mathrm{IL}$ : Output ripple current; ESR: Co equivalent series resistance,
ESL:equivalent series inductance)
※ In selecting a capacitor, make sure the capacitor rating allows sufficient margin relative to output voltage. Note that a lower ESR can minimize output ripple voltage.

Please give due consideration to the conditions in formula (7) below for output capacity, bearing in mind that output rise time must be established within the soft start time frame.

$$
\mathrm{Co} \leqq \frac{3 \mathrm{msec} \times(\text { Limit-IOUT/2) }}{\text { VOUT }} \cdots(7)
$$

Limit: Current Limit Value

Note: Improper capacitor may cause startup malfunctions.
3. Input Capacitor (Cin) Selection


Input Capacitor

The input capacitor selected must have low enough ESR resistance to fully support large ripple output, in order to prevent extreme over current. The formula for ripple current IRMS is given in (8) below.

$$
\mathrm{IRMS}=\frac{\mathrm{lout}^{2}}{2} \times \frac{\sqrt{\mathrm{VOUT}(\mathrm{VIN}-\mathrm{VOUT})}}{\mathrm{VIN}} \quad[\mathrm{~A}] \cdots(8)
$$

Where VIN $=2 \times$ Vout, IRMS $=\frac{\text { IOUT }}{4}$

A low ESR capacitor is recommended to reduce ESR loss and maximize efficiency.
4.MOSFET Selection

Pmain=Pron+Pgate+Ptran
Loss on the main MOSFET

$=\frac{\text { VOUT }}{4 \times \text { VIN }} \quad \times$ RON IOUT $^{2}+$ Ciss $x f \times$ VDD $+\frac{\text { VIN }^{2} \times \text { Crss } \times \text { loutx } f}{2 \times \text { IDRIVE }} \cdots(9)$
(Ron: On-resistance of FET; Ciss: FET gate capacity;
f: Switching frequency Crss: FET inverse transfer function;
IDRIVE: Gate peak current)
Loss on the synchronous MOSFET
Psyn=Pron+Pgate
$=\frac{\text { VIN-VOUT }}{4 \times \text { VIN }} \times$ RON $\times$ IOUT $^{2}+$ Ciss $\times f \times$ VDD


OCP threshold is determined by external OCP setting resistance (RIMAX) and IMAX calculated below.

$$
\begin{gather*}
\text { IIMAX }=\frac{\mathrm{V}_{\mathrm{CS} 1+}-\mathrm{V}_{\mathrm{Cs} 1-}}{250 \mathrm{k} \Omega}+\frac{{\mathrm{V} \mathrm{cs}_{2}+-\mathrm{Vcs}_{2-}}_{250 \mathrm{k} \Omega} \cdot \cdot}{\left(\mathrm{~V}_{\mathrm{CS} 1+}-\mathrm{V}_{\mathrm{CS} 1-}=\mathrm{IL} \times \mathrm{RL} \quad, \mathrm{RL}=\frac{\mathrm{L}}{\mathrm{r} \times \mathrm{C}}\right)} . \tag{11}
\end{gather*}
$$

(RL: the DCR value of coil)
If VIMAX meet the following condition, OCP becomes activated.
$\mathrm{V}_{\text {IMAX }} \leqq \mathrm{l}_{\text {IMAX }} \times \mathrm{R}_{\text {IMAX }}$
(VIMAх: OCP Setting Voltage, $\mathrm{V}_{\text {Iмах }}=1 \mathrm{~V}$ )

7. Setting output voltage

The output voltage is REFIN = VOUT when VOUT is tied to the FB directly. The range of VOUT is $0.4 \mathrm{~V} \sim 3.3 \mathrm{~V}$.


The output voltage is calculated as follows when resistor divider network is connected between the FB and VOUT. REFIN set 5 Vcc . The range of Vout is $0.6 \sim 3.3 \mathrm{~V}$

$$
\begin{equation*}
\text { Vout }=\frac{\mathrm{R} 1+\mathrm{R} 2}{\mathrm{R} 2} \times 0.6[\mathrm{~V}] \cdot \cdots \tag{13}
\end{equation*}
$$


8. Frequency Setting Resistance

The Frequency at steady state is determined by resistance value connected to RT pin.
But actual SW rising time and falling time are factored in due to the external MOSFET gate capacity or switching speed. As a result, On-Time increases.
The frequency is determined by the following formula.

$$
\begin{aligned}
& f[\mathrm{~Hz}]=\frac{\mathrm{VOUT}}{\mathrm{VIN}} \times \frac{1}{\text { Ton }} \cdots(14) \\
& \left(\text { Ton }=\frac{10^{-12} \times \text { REF } \times R_{R T}}{2 \times \text { BUSEN }}+170 \times 10^{-9}\right) \quad \text { Ton : ON TIME }
\end{aligned}
$$

Consequently, total frequency becomes lower than the formula above.
On-Time increases by Dead Time on the condition of zero cross point of inductor current. And also switching frequency increases as the output current increases due to the fixed On-Time and the influence of conduction loss. It is recommended that switching frequency be checked on large current condition (at the point where the inductor current doesn't become reversed from Vout).
9. UVLO

BD95700MUV has function to detect input UVLO voltage in each VCC, 5VCC, and BUSEN for output voltage to start up. If all these inputs go beyond their own UVLO threshold voltage, the soft start function kicks in.
These threshold voltages have their own hysteresis voltage to avoid faulty operation caused by input noises and glitchs.

(Tss: Soft Start Time)

10. Current Phase Balance


BD95700MUV keeps the current phase balance between coil current IL1 and IL2 by controlling the status $\Delta V \operatorname{cs} 1=\Delta V \operatorname{cs} 2$.And for that, it is needed to meet the reference formula below.

$$
\text { L1 = L2 (RL1 =RL2), r1 = r2, C1 = C2. } \quad \cdot \cdot(15)
$$

For detecting the value of $\Delta \mathrm{Vcs} 1$ or $\Delta \mathrm{Vcs} 2$ exactly, it is also needed to meet the formula below.

$$
\mathrm{RL} 1=\frac{\mathrm{L} 1}{\mathrm{r} 1 \times \mathrm{C} 1} \quad \cdots(16)
$$



However, Vcs+ and Vcs- are fed a small current from current sense amplifier, and this current causes a slight difference in the actual value obtained from formula (16). Refer to formula (17) below:
$\Delta \mathrm{Vcs}=\Delta \mathrm{V}-\mathrm{I} \times \mathrm{r} \cdot \cdots(17)$
This difference can be compensated for by adding resistor r 2 .
$\Delta \mathrm{Vcs}=(\Delta \mathrm{V}-\mathrm{I} \mathrm{x})+\mathrm{Ix} \mathrm{r} 2 \cdot \cdots(18)$
To eliminate the difference, choose r 2 to have the same value as r .
$\Delta \mathrm{Vcs}=\Delta \mathrm{V} \cdot \cdots(19)$
11. Vout small Ripple Voltage


Resistor R3 and capacitor C (=56pF)are needed to stabilize switching operation when Vout ripple voltage is less than 20 mV . The values of R1, R2 and R3 are determined as in the formula (20) below

$$
R 1+R 2 \leqq 20 k \Omega, 10 \times R 1 \leqq R 3 \cdots(20)
$$

## Reference Data



Fig1.Sequence


Fig4.Sequence


Fig7.Load Transient Response (VCC=12V)


Fig10.Load Transient Response (VCC=5V)


Fig2.Sequence


Fig5.Sequence


Fig8.Load Transient Response (VCC=12V)


Fig11.Load Transient Response (VCC=8V)


Fig3.Sequence


Fig6.Sequence


Fig9.Load Transient Response (VCC=5V)


Fig12.Load Transient Response (VCC=8V)

## - Reference Data



Fig13.Continuos MODE (VCC=5V)


Fig16.SCP Function


Fig19.Reference Function

Fig22.Current balance ( $\mathrm{lo}=20 \mathrm{~A}$ )



Fig14.Continuos MODE (VCC=8V)


Fig17.SCP Function


Fig20.Frequency range functionally


Fig15.Continuos MODE (VCC=12V)


Fig18.Soft Start


Fig21.Efficiency


Fig23.Current balance ( $\mathrm{Io}=30 \mathrm{~A}$ )


Fig24.Current balance ( $\mathrm{lo}=40 \mathrm{~A}$ )

BD95700MUV Evaluation Board Circuit with 5V Drive (VCC=5V input , VIN=3.3~12V input , REFIN=5VCC, Vout=1.2V )


BD95700MUV Evaluation Board Parts List

| Part No | Value | Company | Part name |
| :---: | :---: | :---: | :---: |
| U1 |  | ROHM | BD95700MUV |
| M2 |  | infineon | BSC119N03SG |
| M3 |  | infineon | BSC119N03SG |
| M4 |  | Infineon | BSC032N03SG |
| M5 |  | Infineon | BSC032N03SG |
| M6 |  | Infineon | BSC119N03SG |
| M7 |  | Infineon | BSC119N03SG |
| M8 |  | Infineon | BSC032N03SG |
| M9 |  | infineon | BSC032N03SG |
| C2 | 10 uF | KYOCERA | CT32X5R106K25A |
| C3 | 1uF | KYOCERA | CM05B105K16A |
| C5 | 1uF | KYOCERA | CM105B105K16A |
| C7 | 10uF | KYOCERA | CM316X5R106M06A |
| C8 | 10uF | KYOCERA | CM21B106M06A |
| C9 | 10uF | KYOCERA | CM21B106M06A |
| C10 | 10uF | KYOCERA | CM21B106M06A |
| C11 | 10uF | KYOCERA | CM21B106M06A |
| C12 | - | - | - |
| C13 | 820uF | SANYO | NC641-643 |
| C14 | 820 uF | SANYO | NC641-643 |
| C15 | 820uF | SANYO | NC641-643 |
| C16 | - | - |  |


| Part No | Value | Company | Part name |
| :---: | :---: | :---: | :---: |
| C17 | - | - | - |
| C18 | 1 uF | KYOCERA | CM05B105K06A |
| C19 | 10 uF | KYOCERA | CT32X5R106K25A |
| C21 | 1 uF | KYOCERA | CM105B105K16A |
| C23 | 0.1 uF | KYOCERA | CM105X5R224K25A |
| C24 | 0.1 uF | KYOCERA | CM105X5R224K25A |
| C25 | 10 uF | KYOCERA | CM316X5R106M10A |
| C27 | 10 uF | KYOCERA | CM316X5R106M06A |
| C28 | 10 uF | KYOCERA | CT32X5R106K25A |
| C31 | 10 uF | KYOCERA | CT32X5R106K25A |
| R2 | $300 \mathrm{k} \Omega$ | ROHM | MCR03 |
| R3 | $30 \mathrm{k} \Omega$ | ROHM | MCR03 |
| R7 | $0 \Omega$ | ROHM | MCR03 |
| R8 | $240 \mathrm{k} \Omega$ | ROHM | MCR03 |
| R9 | $3.6 \mathrm{M} \Omega$ | ROHM | MCR03 |
| R15 | $10 \mathrm{k} \Omega$ | ROHM | MCR03 |
| R16 | $4.87 \mathrm{k} \Omega$ | ROHM | MCR03 |
| R17 | $4.87 \mathrm{k} \Omega$ | ROHM | MCR03 |
| R18 | $10 \mathrm{k} \Omega$ | ROHM | MCR03 |
| R20 | $4.87 \mathrm{k} \Omega$ | ROHM | MCR03 |
| R21 | $4.87 \mathrm{k} \Omega$ | ROHM | MCR03 |
| L1 | 0.47 uH | Cyntec | PCMB105T-R47MS |
| L2 | 0.47 uH | Cyntec | PCMB105T-R47MS |

BD95700MUV Evaluation Board Circuit with 8V Drive (VIN=10.8~13.2V input , REFIN=5VCC, Vout=1.2V )


BD95700MUV Evaluation Board Parts List

| Part No | Value | Company | Part name |
| :---: | :---: | :---: | :---: |
| U1 |  | ROHM | BD95700MUV |
| M2 |  | infineon | BSC119N03SG |
| M3 |  | infineon | BSC119N03SG |
| M4 |  | Infineon | BSC032N03SG |
| M5 |  | Infineon | BSC032N03SG |
| M6 |  | Infineon | BSC119N03SG |
| M7 |  | Infineon | BSC119N03SG |
| M8 |  | Infineon | BSC032N03SG |
| M9 |  | infineon | BSC032N03SG |
| C2 | 10uF | KYOCERA | CT32X5R106K25A |
| C3 | 1uF | KYOCERA | CM05B105K16A |
| C5 | 1uF | KYOCERA | CM105B105K16A |
| C7 | 10uF | KYOCERA | CM316X5R106M06A |
| C8 | 10uF | KYOCERA | CM21B106M06A |
| C9 | 10uF | KYOCERA | CM21B106M06A |
| C10 | 10uF | KYOCERA | CM21B106M06A |
| C11 | 10uF | KYOCERA | CM21B106M06A |
| C12 | - | - | - |
| C13 | 820uF | SANYO | NC641-643 |
| C14 | 820uF | SANYO | NC641-643 |
| C15 | 820uF | SANYO | NC641-643 |
| C16 | - | - | - |
| C17 | - | - | - |


| Part No | Value | Company | Part name |
| :---: | :---: | :---: | :---: |
| C18 | 1 uF | KYOCERA | CM05B105K06A |
| C19 | 10 uF | KYOCERA | CT32X5R106K25A |
| C21 | 1 uF | KYOCERA | CM105B105K16A |
| C23 | 0.1 uF | KYOCERA | CM105X5R224K25A |
| C24 | 0.1 uF | KYOCERA | CM105X5R224K25A |
| C25 | 10 uF | KYOCERA | CM316X5R106M10A |
| C27 | 10 uF | KYOCERA | CM316X5R106M06A |
| C28 | 10 uF | KYOCERA | CT32X5R106K25A |
| C31 | 10 uF | KYOCERA | CT32X5R106K25A |
| R1 | $10 \mathrm{k} \Omega$ | ROHM | MCR03 |
| R2 | $300 \mathrm{k} \Omega$ | ROHM | MCR03 |
| R3 | $30 \mathrm{k} \Omega$ | ROHM | MCR03 |
| R7 | $0 \Omega$ | ROHM | MCR03 |
| R8 | $240 \mathrm{k} \Omega$ | ROHM | MCR03 |
| R9 | $3.6 \mathrm{M} \Omega$ | ROHM | MCR03 |
| R15 | $10 \mathrm{k} \Omega$ | ROHM | MCR03 |
| R16 | $4.87 \mathrm{k} \Omega$ | ROHM | MCR03 |
| R17 | $4.87 \mathrm{k} \Omega$ | ROHM | MCR03 |
| R18 | $10 \mathrm{k} \Omega$ | ROHM | MCR03 |
| R20 | $4.87 \mathrm{k} \Omega$ | ROHM | MCR03 |
| R21 | $4.87 \mathrm{k} \Omega$ | ROHM | MCR03 |
| L1 | 0.47 uH | Cyntec | PCMB105T-R47MS |
| L2 | 0.47 uH | Cyntec | PCMB105T-R47MS |

BD95700MUV Evaluation Board Circuit with 12V Drive ( VIN=12V input, VCC=12V input, REFIN=5VCC, Vout=1.2V )


BD95700MUV Evaluation Board Parts List

| Part No | Value | Company | Part name |
| :---: | :---: | :---: | :---: |
| U1 |  | ROHM | BD95700MUV |
| M2 |  | infineon | BSC119N03SG |
| M3 |  | infineon | BSC119N03SG |
| M4 |  | Infineon | BSC032N03SG |
| M5 |  | Infineon | BSC032N03SG |
| M6 |  | Infineon | BSC119N03SG |
| M7 |  | Infineon | BSC119N03SG |
| M8 |  | Infineon | BSC032N03SG |
| M9 |  | infineon | BSC032N03SG |
| C2 | 10 uF | KYOCERA | CT32X5R106K25A |
| C3 | 1 uF | KYOCERA | CM05B105K16A |
| C5 | 1uF | KYOCERA | CM105B105K16A |
| C7 | 10uF | KYOCERA | CM316X5R106M06A |
| C8 | 10uF | KYOCERA | CM21B106M06A |
| C9 | 10uF | KYOCERA | CM21B106M06A |
| C10 | 10uF | KYOCERA | CM21B106M06A |
| C11 | 10uF | KYOCERA | CM21B106M06A |
| C12 | - | - | - |
| C13 | 820uF | SANYO | NC641-643 |
| C14 | $820 u F ~$ | SANYO | NC641-643 |
| C15 | 820uF | SANYO | NC641-643 |
| C16 | - | - | - |


| Part No | Value | Company | Part name |
| :---: | :---: | :---: | :---: |
| C17 | - | - | - |
| C18 | 1 uF | KYOCERA | CM05B105K06A |
| C19 | 10 uF | KYOCERA | CT32X5R106K25A |
| C21 | 1 uF | KYOCERA | CM105B105K16A |
| C23 | 0.1 uF | KYOCERA | CM105X5R224K25A |
| C24 | 0.1 uF | KYOCERA | CM105X5R224K25A |
| C25 | 10 uF | KYOCERA | CM316X5R106M10A |
| C27 | 10 uF | KYOCERA | CM316X5R106M06A |
| C28 | 10 uF | KYOCERA | CT32X5R106K25A |
| C31 | 10 uF | KYOCERA | CT32X5R106K25A |
| R2 | $300 \mathrm{k} \Omega$ | ROHM | MCR03 |
| R3 | $30 \mathrm{k} \Omega$ | ROHM | MCR03 |
| R7 | $0 \Omega$ | ROHM | MCR03 |
| R8 | $240 \mathrm{k} \Omega$ | ROHM | MCR03 |
| R9 | $3.6 \mathrm{M} \Omega$ | ROHM | MCR03 |
| R15 | $10 \mathrm{k} \Omega$ | ROHM | MCR03 |
| R16 | $4.87 \mathrm{k} \Omega$ | ROHM | MCR03 |
| R17 | $4.87 \mathrm{k} \Omega$ | ROHM | MCR03 |
| R18 | $10 \mathrm{k} \Omega$ | ROHM | MCR03 |
| R20 | $4.87 \mathrm{k} \Omega$ | ROHM | MCR03 |
| R21 | $4.87 \mathrm{k} \Omega$ | ROHM | MCR03 |
| L1 | 0.47 uH | Cyntec | PCMB105T-R47MS |
| L2 | 0.47 uH | Cyntec | PCMB105T-R47MS |

## - Operation Notes

1. Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.
2. Connecting the power supply connector backward

Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.
3. Power supply lines

Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, not that capacitance characteristic values are reduced at low temperatures.
4. GND voltage

The potential of GND pin must be minimum potential in all operating conditions.
5. Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation ( Pd ) in actual operating conditions.
6. Inter-pin shorts and mounting errors

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.
7. Actions in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.
8. ASO

When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.
9. Thermal shutdown circuit

The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

|  | TSD on temperature [ $\left.{ }^{\circ} \mathrm{C}\right]$ (typ.) | Hysteresis temperature [ $\left.{ }^{\circ} \mathrm{C}\right]$ (typ.) |
| :---: | :---: | :---: |
| BD95700MUV | 175 | 15 |

10. Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.
11. Regarding input pin of the IC

This monolithic IC contains $\mathrm{P}+$ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these $P$ layers with the $N$ layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.
Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

12. Ground Wiring Pattern

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

## Power Dissipation



Fig. 25 Thermal derating curve
(VQFNO20V4040)

- Type Designations (Selections) for Ordering


Part No.


Part No.


Package MUV : VQFN024V4040


Packaging and forming specification E2: Embossed tape and reel

## VQFN024V4040



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